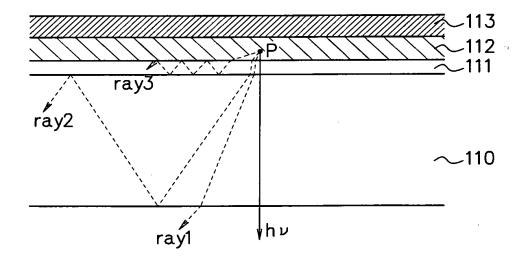
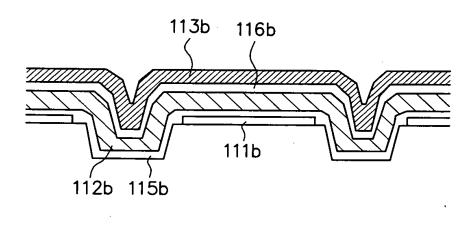
F I G. 1 PRIOR ART

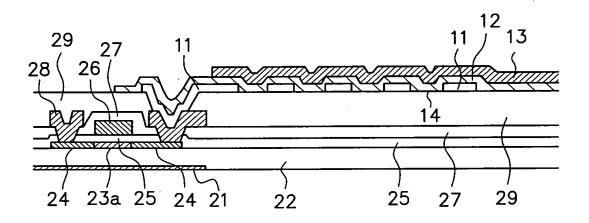


F I G. 2 PRIOR ART

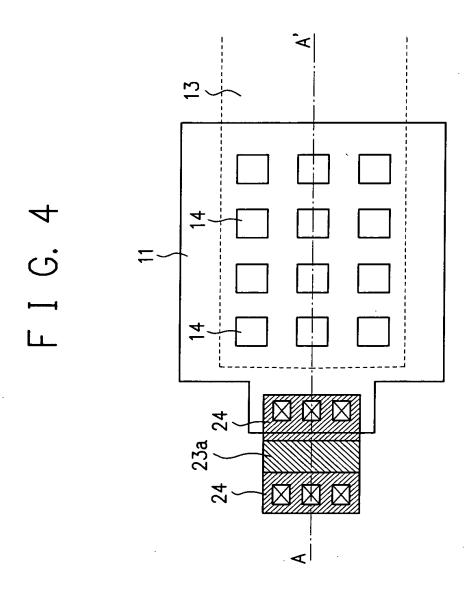


11_.0b

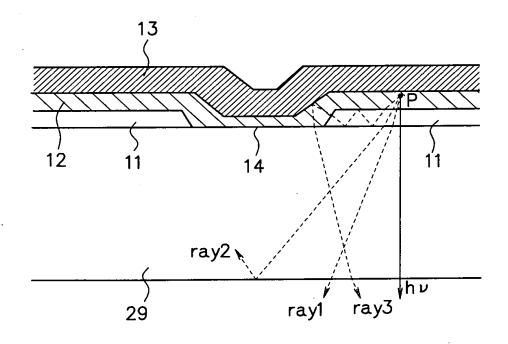
F I G. 3



10



F I G. 5

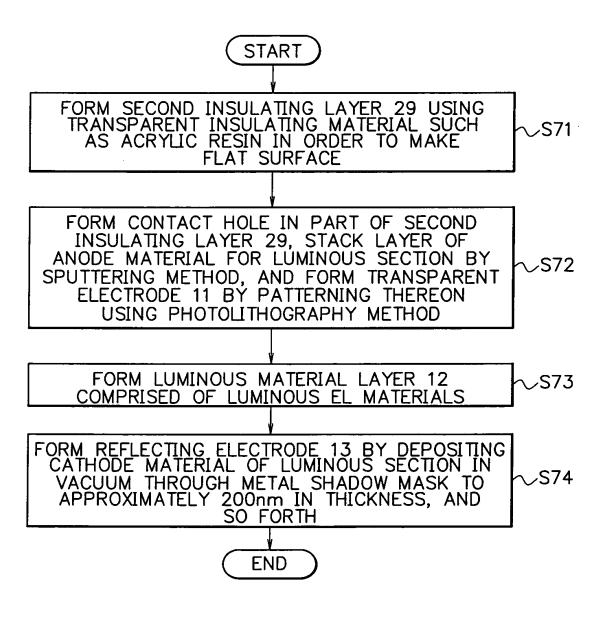


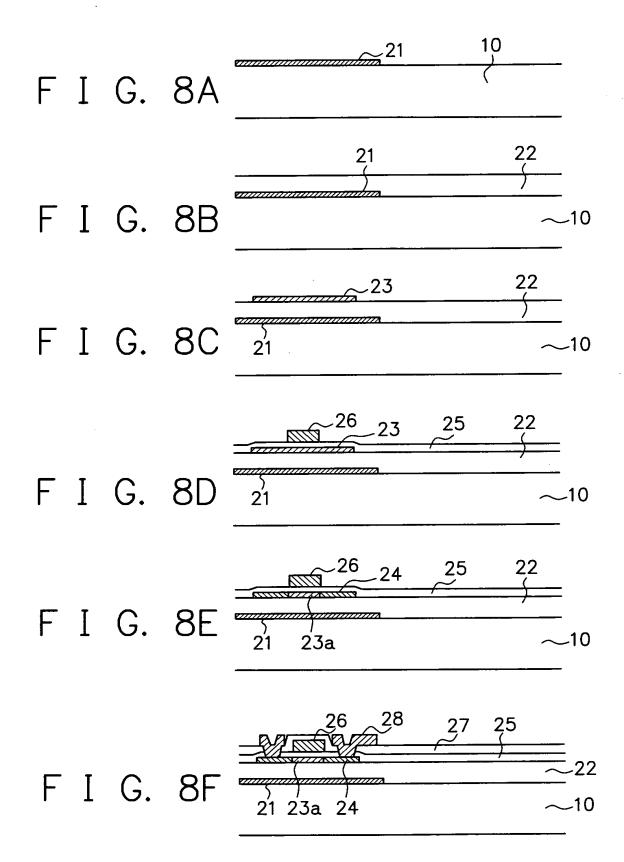
F I G. 6

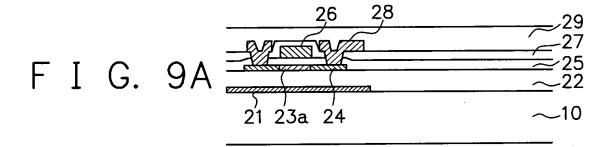
START FORM LIGHT SHIELDING LAYER 21 BY PATTERNING MATERIAL(S) HAVING HIGH MELTING POINT SUCH AS ∨S61 TUNGSTEN SILICIDE ON TRANSPARENT SUBSTRATE 10 SUCH AS GLASS STACK BARRIER LAYER 22 OF SiO2 ALL ∿S62 OVER SURFACES AFTER FORMING AMORPHOUS SI (a-Si) LAYER ON BARRIER LAYER 22, TRANSFORM THE a-Si LAYER \sim S63 INTO poly-Si LAYER BY IRRADIATING PULSED LIGHT THEREON, AND FORM THIN FILM SEMICONDUCTOR 23 BY PATTERNING THE poly—Si LAYER STACK SiO2 LAYER APPROXIMATELY 50nm THICK AND WSI LAYER APPROXIMATELY 200nm THICK ALL ÖVER SÚRFACÉS, AND FORM GATE INSULATING LAYER 25 AND GATE ELECTRODE 26 BY PATTERNING √S64 THE WSI LAYER IMPLANT PHOSPHOROUS(P) OR BORON(B) HEAVILY TO SELECTED REGION OF THIN FILM SEMICONDUCTOR 23 BY ION DOPING METHOD AND SO FORTH, ACTIVATE THE IMPLANTED IMPURITY ELEMENT BY HEATING SUBSTRATE TO APPROXIMATELY 500°C, AND FORM SOURCE/DRAIN REGION 24 AND CHANNEL REGION 23a \sim S65STACK FIRST INSULATING LAYER 27 SUCH AS SiO2 ALL OVER SURFACES BY PLASMA CVD METHOD AND SO FORTH, MAKE CONTACT HOLES, AND FORM SOURCE/DRAIN ELECTRODE 28 AND WIRING WITH ∨S66 LOW-RESISTANCE METAL MATERIAL

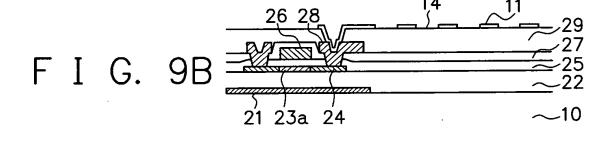
END

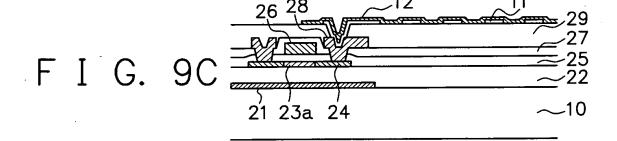
F I G. 7

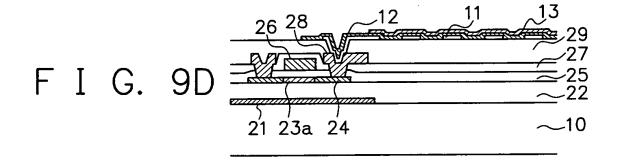




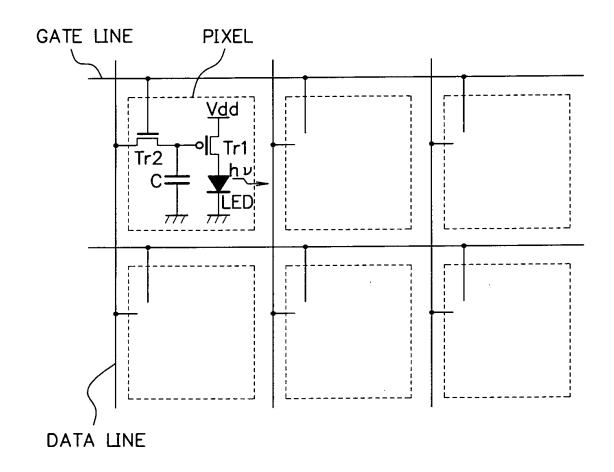




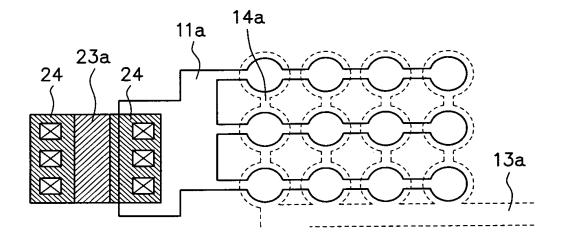




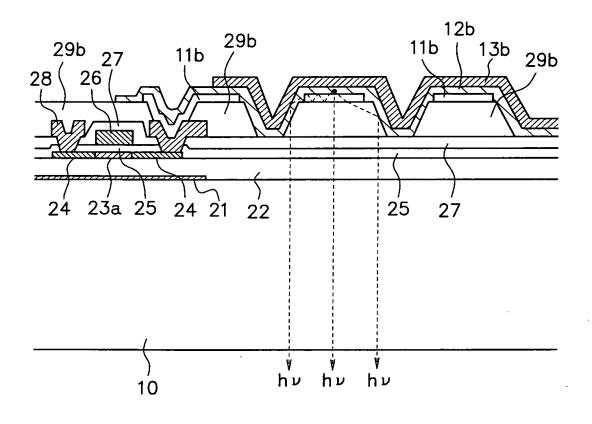
F I G. 10



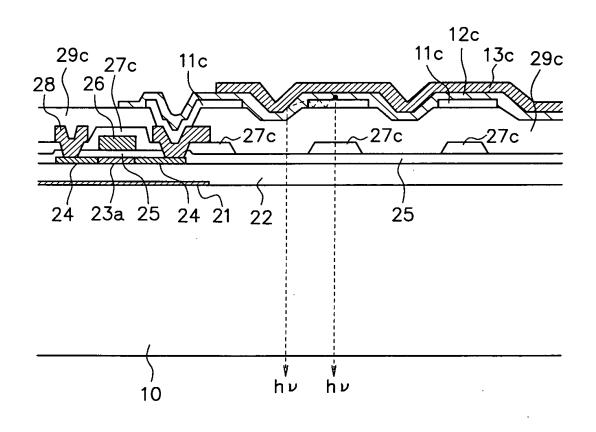
F I G. 11



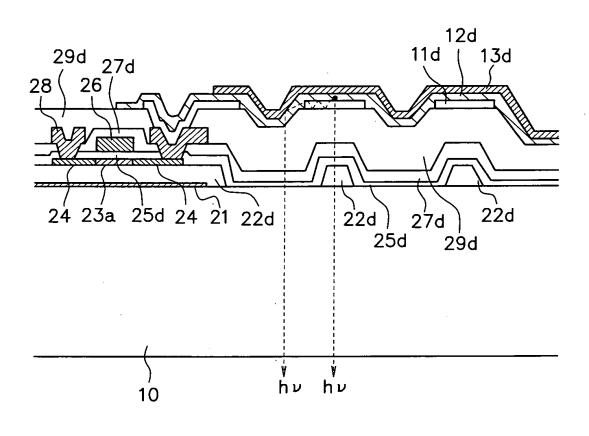
F I G. 12



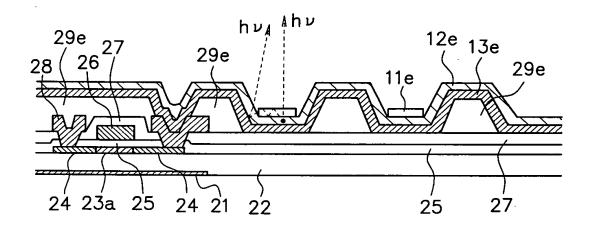
F I G. 13



F I G. 14



F I G. 15



10f

F I G. 16

